REMARKS

Claims 27-46 and 72, 73 and 75-95 are pending in the present application. Claims 27, 36, 72, 73 and 87 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

Claims 27-46 and 72-95 stand rejected under 35 U.S.C. 112, second paragraph. The Applicant notes that claim 74 is cancelled.

The Office Action indicates at page 3 paragraph 1 that in claims 27 and 72 the limitation "an epitaxial layer...extending from the gate dielectric layer in a horizontal direction substantially parallel to the substrate" is not clear. Claims 27 and 72 are amended to recite "an epitaxial layer...extending from the gate dielectric layer substantially parallel to the substrate in a horizontal direction". This makes it clear that the epitaxial layer extends substantially parallel to the substrate. As stated in the Office Action, at page 3, lines 11-15, this limitation, stated this way defines over the Nishiyama reference.

The Office Action further indicates at page 3, paragraph 2, that in claim 27 the limitation "insulating sidewall spacers" is not clear. Such insulating sidewall spacers are traditionally formed at the side walls of semiconductor structures by applying an insulating film that is later etched using anisotropic etching, or a dry etch process, so that remnants of the insulating film remain at the sidewalls of the structures. An example of this process is provided in the present specification at page 17, lines 1-5, describing, in this example, the formation of insulating sidewall spacers 316, 318. In Nishiyama, spacers 208 are considered gate sidewall spacers in this sense, but void-filling insulative regions 215 would not be considered sidewall spacers. The void-filling insulative regions instead are applied as a fill layer that fills the void between the spacers 208 at the side walls of the Nishiyama gate and other nearby structures.

The Office Action further indicates at page 4, paragraph 1, that in claim 27 the limitation "sidewall spacers having bottom portions on the first source/drain regions" is unclear. Claim 27 is amended to recite "insulating sidewall spacers on the first source/drain regions in the epitaxial layer at upper side portions of the gate electrode, bottom surfaces of the insulating sidewall spacers extending from the upper side portions of the gate electrode substantially parallel to the substrate." It should now be clear that the insulating sidewall spacers of claim 27 are "on" the "first source/drain regions" that are in the "epitaxial layer", which epitaxial layer, as stated above, extends from the gate dielectric layer substantially parallel to the substrate, and which source/drain regions are located in the epitaxial layer at lower side portions of the gate electrode. Therefore, it should now be clear that the bottom surfaces of the insulating sidewall spacers are substantially parallel to the substrate. Thus, in the present invention as claimed in claim 27, the insulating sidewall spacers, bottom surfaces of which extend from the upper side portions of the gate electrode are on the underlying first source/drain regions formed in an epitaxial layer at lower side portions of the gate electrode. Nishiyama does not teach or suggest this feature, since, in Nishiyama, the sidewall spacers 208 lie directly on an upper surface of the Nishiyama substrate 202.

The Office Action further indicates at page 4, paragraph 2, that in claim 72 the limitation "a gate dielectric layer includes...vertical portions that extend along lower side portions of the gate electrode" is unclear. Claim 72 is amended to recite a "gate dielectric layer includes...side portions that extend in a vertical direction along the lower side portions of the gate electrode". In the present invention as claimed in claim 72, the "gate dielectric layer" is formed of the "horizontal portion" that is the portion that insulates the gate electrode from the portion of the channel region formed in an upper part of the substrate, and is formed of the side portions that insulate the gate electrode from the portion of the channel region formed in the epitaxial layer. It should now be clear what is meant by the "side portions" of the gate dielectric layer. In contrast, the gate sidewalls 208 of Nishiyama do not insulate the gate from a channel region, and therefore, the Nishiyama gate sidewalls 208 are not a gate dielectric layer, as claimed.

Entry of the amendments and reconsideration and removal of the rejections under 35 U.S.C. 112, second paragraph, are respectfully requested.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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